

# Rekha R

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I am a Post Doctoral Fellow in Computer Science and Automation at IISc Bangalore.  
My current research interest is in Program Analysis for Verification.

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## Education

- 2009–2017 **Ph.D**, *National Institute of Technology Calicut*, Kerala, India.  
2007–2009 **M.Tech in Computer Science and Engineering**, *National Institute of Technology Calicut*, Kerala, India, *CGPA: 9.48* (Out of 10) .  
1998–2002 **B.Tech in Computer Science and Engineering**, *Kerala University*, Kerala, India,  
*First Class with Distinction*.

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## Research

Area of interest Program Analysis for Verification

Current work “Static Race Detection for Embedded Systems”

Embedded systems are increasingly employed in safety-critical situations and the presence of races may lead to erroneous behaviour with serious consequences. Hence detection of races is a step towards proving correctness of programs. Two statements are involved in a *data race* if they are conflicting accesses to a shared memory location and can happen “simultaneously” or one after another. The problem of detection of races has been well studied for classical concurrent systems which has standard synchronization techniques and thread interleaving semantics. Embedded systems typically use non-standard synchronization mechanisms like disabling and enabling interrupts, suspending and resuming scheduler or specific threads, dynamically raising and lowering thread priorities, use of flags, etc. in addition to the standard locks. This brings in complex context switching possibilities which makes it challenging to detect races with high precision. I proposed a new definition of race and notion of *disjoint blocks* that enables a principled approach to detect races in such systems as well. The new definition and notions are generic enough that it applies to various classes of programs.

PhD Thesis “Detection of redundant expressions in SSA”

Elimination of redundant expressions in a program, based on values of expressions, is a compiler optimization done with a view to improve on the runtime efficiency of the program. The problem is complex enough to warrant a separation of the analysis and the optimization phases. The problem studied in detail for my PhD thesis is the detection of redundant expressions. An expression  $e$  is *redundant* if its value has already been computed. The problem is well studied but the state-of-art algorithms are either “precise” or polynomial-time computable but not both. The new perspectives on *confluence operation* and *values*, introduced in the thesis, has enabled combining precision with polynomial time computability. I proposed and implemented two algorithms to detect redundant expressions in Static Single Assignment (SSA) form of programs. The algorithms uses the novel concepts of *value  $\phi$ -function* and  *$\phi$ -value*. One of the algorithms was adopted as an analysis pass in LLVM (v5.0.0) compiler by their principal developer Daniel Berlin.

Masters Thesis “Partial Redundancy Elimination”

Partial Redundancy Elimination is a compiler optimization that eliminates expressions that are redundant on some but not necessarily all paths in a program. I proposed an algorithm to eliminate partially redundant expressions in programs. The algorithm uses only three uni-directional analyses.

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## Experience

I have over three years of research experience after doctoral study. I also have over 4½ years of experience as a full time teacher and 5 years as a teaching assistant during graduate studies and post doctoral work.

### Research Associate

Oct 2018 – current UGC-Dr. DS Kothari Post Doctoral Fellow with Prof. Deepak D’Souza at Computer Science and Automation, IISc Bangalore.

Jul 2017 – Research Associate with Prof. Deepak D’Souza at Computer Science and Automation, IISc Bangalore.  
Oct 2018

### Teaching Assistant

2018–2020 Indian Institute of Science Bangalore

+ Assisted in the “Program Synthesis and Machine Learning” course. This course introduces the fundamentals of program synthesis and ML. Various methods to use the ideas of ML in program synthesis were explored through paper discussions. I assisted a doctoral student with his course project on “Improving Semantic Code Search Using Abstract Tree Based Representation”. 2020

+ Delivered lecture on “Kildall’s Algorithm for Data Flow Analysis” for graduate students. Also assisted in the evaluation of course project in the Java based WALA framework. 2018

- 2009–2013 National Institute of Technology Calicut
- + Delivered lectures on “Foundations of Data Flow Analysis” for graduate students. The lectures are based on the text book “Compilers: Principles, Techniques, and Tools” by Aho, Lam, Sethi, and Ullman. 2011, 2012
  - + Designed and assisted in Programming Lab for undergraduates. This lab course introduced techniques to control intellectual complexity of programs - in particular, procedural abstraction, data abstraction, and modular design. The course is based on the textbook “Structure and Interpretation of Computer Programs” by Gerald Jay Sussman and Hal Abelson. 2011, 2012
  - + Assisted in Compiler Lab for undergraduates. This lab course involved implementation of a Simple Intermediate Language (SIL) designed in-house for the purpose. 2010, 2013
  - + Designed and assisted in Programming Languages Lab for undergraduates. This lab involved implementation of Untyped and Typed Lambda Calculus and its variants, based on the textbook “Types and Programming Languages” by Benjamin C Pierce. The interpreter for these languages are written in *OCaml*. 2010, 2011, 2012

### Lecturer

- Sept **College of Engineering, Perumon**, Kerala, India.  
 2006–July Offered courses on Computer Networks and E-commerce for undergraduates.  
 2007
- Feb **College of Engineering, Vadakara (formerly Co-operative Institute of Technology Vadakara)**, Calicut, Kerala, India.  
 2004–Aug Offered courses on Design and Analysis of Algorithms and Software Engineering for undergraduates.  
 2006

### Lecturer on Ad hoc Basis

- Dec **College of Engineering, Perumon**, Kerala, India.  
 2002–Feb Offered courses on E-commerce and Software Engineering for undergraduates.  
 2004

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## Publications

- Pai R.**, Singh A., D’Souza D., D’Souza M., Prakash P. Static Analysis for Detecting High-Level Races in RTOS Kernels. Formal Methods of Software Design (FMSD) 2021 (online). IF: 0.673
- Tulsyan R., **Pai R.**, D’Souza D. Static Race Detection for RTOS Applications. In: Saxena N. and Simon S. (eds) 40<sup>th</sup> IARCS Foundations of Software Technology and Theoretical Computer Science (FSTTCS) 2020. LIPIcs vol 182, pp.1–20, Schloss Dagstuhl
- Singh A., **Pai R.**, D’Souza D., D’Souza M. Static Analysis for Detecting High-Level Races in RTOS Kernels. In: ter Beek M., McIver A., Oliveira J. (eds) Formal Methods – The Next 30 Years. FM 2019. Lecture Notes in Computer Science, vol 11800, pp.337–353. Springer, Cham
- Chopra N., **Pai R.**, D’Souza D. Data Races and Static Analysis for Interrupt-Driven Kernels. In: Caires L. (eds) Programming Languages and Systems. ESOP 2019. Lecture Notes in Computer Science, vol 11423, pp.697–723. Springer, Cham

**Pai, Rekha R.** Detection of Redundant Expressions: A Precise, Efficient, and Pragmatic Algorithm in SSA. *Computer Languages, Systems, and Structures*, 2016. vol 46, pp.167–181. IF: 0.5

**Pai, Rekha R.** Detection of Redundant Expressions: A Complete and Polynomial-time Algorithm in SSA. In the Proceedings of Asian Symposium of Programming Languages and Systems (APLAS) 2015. LNCS 9458, pp. 49–65, Springer International Publishing Switzerland

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## Workshops/Schools Attended (recent)

The Fourth International Programming Language Implementation Summer School (PLISS), an online event. May – June, 2021.

Workshop on Research Highlights in Programming Languages co-located with 40<sup>th</sup> IARCS Annual Conference on Foundations of Software Technology and Theoretical Computer Science (FSTTCS) 2020 (online event). December 15 – 17, 2020.

Winter School in Software Engineering, TRDDC Pune, India. December 11 – 16, 2017.

The Second Indian SAT+SMT School, Infosys Campus, Mysore, India. December 6 – 8, 2017.

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## Professional Service (selected)

Program Committee member of the 8<sup>th</sup> Workshop on Advances in Programming Languages, 2 – 5 September, 2021, online.

Program Committee member of the 7<sup>th</sup> Workshop on Advances in Programming Languages, 1 – 4 September, 2019, Leipzig, Germany.

Research Affairs Secretary of NIT Calicut ACM Student Chapter, 2013.

Volunteered for International Symposium on Bio-Computing (ISB 2010), jointly organised by NIT Calicut and Indiana University Purdue University Indianapolis in cooperation with ACM held at Calicut, Kerala.

Faculty-in-charge of Indian Society for Technical Education (ISTE) Student's Chapter at College of Engineering Perumon, 2006 – 2007.

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## Achievements

UGC-Dr. DS Kothari Post Doctoral Fellowship for the period 2018-21

SERB-National Post Doctoral Fellowship for the period 2018-20

National Eligibility Test (NET) qualified for Assistant Professor position

ACM-Women Scholarship for attending APLAS'15 held at Pohang, South Korea, 2015

ACM-India/IARCS Travel Grant for attending APLAS'15 held at Pohang, South Korea, 2015

MHRD Government of India PhD Scholarship 2009-2013

MHRD Government of India Graduate Aptitude Test in Engineering (GATE) Scholarship 2007-2009

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## Talks (recent)

Delivered a lecture on *Static Race Detection in Embedded Systems* in the Workshop on Research Highlights in Programming Languages co-located with 40<sup>th</sup> IARCS Annual Conference on Foundations of Software Technology and Theoretical Computer Science (FSTTCS) 2020.

Delivered a lecture in the *TeQIP* Phase-II Faculty Development Programme on *Syntax Directed Translation* at College of Engineering Perumon on April 2016.

Delivered a lecture in the *TeQIP* Phase-II Faculty Development Programme on *Program Analysis and Transformation* at College of Engineering Thalassery on December 2015.

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## References

Deepak D'Souza,  
Professor,  
Department of Computer Science and Automation  
Indian Institute of Science Bangalore, India.  
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Vineeth Paleri,  
Professor,  
Department of Computer Science and Engineering  
National Institute of Technology Calicut. Kerala, India.  
vpaleri@nitc.ac.in