

Kartik Nagar

PERSONAL PARTICULARS

Compiler Lab,
Department of Computer Science and Automation (CSA),
Indian Institute of Science,
Bangalore, India.
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EDUCATION

Indian Institute of Science, Bangalore **Aug 2012 - present**
Ph.D. Computer Science, Department of CSA, IISc.

- Thesis : Precise analysis of private and shared caches for tight WCET estimates.
- Advisor : Professor Y.N. Srikant
- CGPA : 7/8

Indian Institute of Science, Bangalore **Aug 2010 - July 2012**
M.E. Computer Science, Department of CSA, IISc.

- Thesis : Cache analysis for multi-level data caches.
- Advisor : Professor Y.N. Srikant
- CGPA : 7.4/8

Dhirubhai Ambani Institute of Information and Communication Technology, Gandhinagar **Aug 2006 - July 2010**
B.Tech. Information and Communication Technology, DAIICT.

- CGPA : 9.94/10

RESEARCH INTERESTS

Program Analysis, Formal Methods of Verification, Real-time Systems.

PUBLICATIONS

Journal Papers

- [TECS] *Fast and Precise Worst Case Interference Placement for Shared Cache Analysis*. Kartik Nagar and Y.N. Srikant. Accepted in ACM Transactions on Embedded Computing Systems, 2015.

Conference Papers

- [VMCAI] *Path sensitive cache analysis using cache miss paths*. Kartik Nagar and Y.N. Srikant. 16th International Conference on Verification, Model Checking, and Abstract Interpretation (VMCAI), 2015.
- [RTAS] *Precise shared cache analysis using optimal interference placement*. Kartik Nagar and Y.N. Srikant. 20th IEEE Real Time and Embedded Technology and Applications Symposium (RTAS), 2014.
- [MEMOCODE] *Interdependent cache analyses for better precision and safety*. Kartik Nagar and Y.N. Srikant. 10th ACM/IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE), 2012.

TALKS

- *Path sensitive cache analysis using cache miss paths*, International Conference on Verification, Model Checking, and Abstract Interpretation (VMCAI) 2015, Mumbai, India, January 2015.
- *Data flow Analysis*, CSA Undergraduate Summer School on Computer Science, IISc, Bangalore, June 2014.
- *Precise shared cache analysis using optimal interference placement*, IEEE Real Time and Embedded Technology and Applications Symposium (RTAS), Berlin, Germany, April 2014.
- *A Comprehensive cache analysis for multi-level caches*, IMPECS-CSA Workshop on Program Analysis, Indian Institute of Science, Bangalore, September 2012.
- *Interdependent cache analyses for better precision and safety*, ACM/IEEE International Conference on Formal Methods and Models for Codesign (MEM-OCODE) Arlington, Virginia, USA, July 2012.

GRADUATE COURSES

- Operating Systems
- Program Analysis and Verification
- Compiler Design
- Graph Theory
- Design and Analysis of Algorithms
- Machine Learning

AWARDS AND HONORS

- Awarded Microsoft Research India PhD fellowship, 2013.
- Secured an all India rank of 19 (out of around 100,000 candidates) in Graduate Aptitude Test in Engineering (GATE) 2010.
- Gold medal for first rank in B.Tech., DAIICT, Gandhinagar, 2011.

TEACHING EXPERIENCE

Teaching Assistant for ‘Algorithms and Programming’ (Aug-Dec 2014), ‘Compiler Design’ (Jan-Apr 2013), ‘Program Analysis and Verification’ (Aug-Dec 2012) at Indian Institute of Science, Bangalore.

SKILLS

Languages : English (fluent), Gujarati (Native), Hindi.
Programming : C/C++, Java, Latex, Shell programming.

REFERENCES

Available upon request.